CLAIMS

1. An amplifier (1) comprising a first (10) and a second (20) interconnected transistor and an associated dynamic biasing circuit (100), **characterized in that** said dynamic biasing circuit (100) comprises:

- means for generating (110) a dynamic bias signal based on detection of a direct current (DC) signal of said first transistor (10); and
- means for applying (120) said dynamic bias signal to said second transistor (20).

2. The amplifier according to claim 1, **characterized in that** said DC signal is a DC current for said first transistor (10).

3. The amplifier according to claim 1 or 2, **characterized in that** said first transistor (10) having an input electrode (12) adapted for receiving an input signal and an output electrode (16) connected to an input terminal of said dynamic biasing circuit (100) and to an input electrode (22) of said second transistor (20), said dynamic biasing circuit (100) having an output terminal connected to said input electrode (22) of said second transistor (20), and said second transistor (20) having an output electrode (26) adapted for providing an output signal.

4. The amplifier according to claim 1 or 2, **characterized in that** an input electrode (12; 22) of said first transistor (10) and of said second transistor (20) is adapted for receiving an input signal and an output electrode (16; 26) of said first transistor (10) and of said second transistor (20) is adapted for providing an output signal, said dynamic biasing circuit (100) having an input terminal connected to said output electrode (16) of said first transistor (10) and an output terminal connected to said input electrode (22) of said second transistor (20).

5. The amplifier according to claim 1 or 2, **characterized in that** said bias signal generating means (110) is arranged for detecting a voltage drop caused

by said DC signal and for generating said dynamic bias signal based on said detected voltage drop.

6. The amplifier according to claim 5, **characterized in that** said dynamic biasing circuit (100) comprises:

- resistance means (130) connected to an output electrode (16) of said first transistor (10) and arranged for connection with a supply voltage (3); and
- an operation amplifier (140) having a first input terminal (142) connected to said output electrode (16) of said first transistor (10), a second input terminal (144) for connection with said first supply voltage (3) and an output terminal (146) connected to an input electrode (22) of said second transistor (20), said operational amplifier (140) is adapted for detecting said voltage drop as a difference between a first input voltage of said first input terminal (142) and a second input voltage of said second input terminal (144).

7. The amplifier according to claim 6, **characterized in that** said operational amplifier (140) is adapted for generating an output voltage signal proportional to said detected voltage drop, said dynamic bias signal comprising said output voltage signal.

8. The amplifier according to claim 5, **characterized in that** said dynamic biasing circuit (100) comprises:

- resistance means (130) connected to an output electrode (16) of said first transistor (10) and arranged for connection with a supply voltage (3); and
- a third transistor (150) having an input terminal arranged for connection with said supply voltage (3) and an output electrode connected to said output electrode (16) of said first transistor (10) and to an input electrode (22) of said second transistor (20), said third transistor (150) detecting said voltage drop as a difference between a first input voltage of said input electrode and a second input voltage of said output electrode.

9. The amplifier according to any of the claims 1 to 8, **characterized by** a fourth transistor (160) connected to said applying means (140) and adapted for adjusting said dynamic bias signal for said second transistor (20).

10. The amplifier according to any of the claims 1 to 9, **characterized by** a fifth transistor (30) cascade connected to said first transistor (10), said applying means (140) is configured for applying said dynamic bias signal to said fifth transistor (30).

11. The amplifier according to claim 10, **characterized by**:

- a first voltage dividing circuit (162,164) having an input terminal connected to said applying means (140) and an output terminal connected to said second transistor (20); and
- a second voltage dividing circuit (172,174) having an input terminal connected to said applying means (140) and an output terminal connected to said fifth transistor (30).

12. A dynamic biasing circuit (100) for biasing an amplifier (1) comprising a first transistor (10) and a second (20) interconnected transistor, **characterized by**:

- means for generating (110) a dynamic bias signal based on detection of a direct current (DC) signal of said first transistor (10); and
- means for applying (120) said dynamic bias signal to said second transistor (20).

13. The circuit according to claim 12, **characterized in that** said DC signal is a DC current for said first transistor (10).

14. The circuit according to claim 12 or 13, **characterized in that** bias signal generating means (110) is arranged for detecting a voltage drop caused by said DC signal and for generating said dynamic bias signal based on said detected voltage drop.

15. The circuit according to claim 14, **characterized in that** said dynamic biasing circuit (100) comprises:

- resistance means (130) connected to an output electrode (16) of said first transistor (10) and arranged for connection with a supply voltage (3); and
- an operation amplifier (140) having a first input terminal (142) connected to said output electrode (16) of said first transistor (10), a second input terminal (144) for connection with said first supply voltage (3) and an output terminal (146) connected to an input electrode (22) of said second transistor (20), said operational amplifier (140) detecting said voltage drop as a difference between a first input voltage of said first input terminal (142) and a second input voltage of said second input terminal (144).

16. The circuit according to claim 15, **characterized in that** said operational amplifier (140) is adapted for generating an output voltage signal proportional to said detected voltage drop, said dynamic bias signal comprising said output voltage signal.

17. The circuit according to claim 14, **characterized in that** said dynamic biasing circuit (100) comprises:

- resistance means (130) connected to an output electrode (16) of said first transistor (10) and arranged for connection with a supply voltage (3); and
- a third transistor (150) having an input terminal arranged for connection with said supply voltage (3) and an output electrode connected to said output electrode (16) of said first transistor (10) and to an input electrode (22) of said second transistor (20), said third transistor (150) detecting said voltage drop as a difference between a first input voltage of said input electrode and a second input voltage of said output electrode.

18. The circuit according to any of the claims 12 to 17, **characterized by** a fourth transistor (160) connected to said applying means (140) and adapted for adjusting said dynamic bias signal for said dynamically biasing circuit (100).

19. A method for dynamically biasing an amplifier (1) comprising a first transistor (10) and a second (20) interconnected transistor, the method comprises applying an input signal to said first transistor (10),
characterized by the steps of:

- generating a dynamic bias signal based on detection of a direct current (DC) signal of said first transistor (10); and
- applying said dynamic bias voltage signal to of said second transistor (20).

20. The method according to claim 19, **characterized in that** said DC signal is a DC current for said first transistor (10).

21. The method according to claim 19 or 20, **characterized in that** said bias signal generating step comprises the steps of:

- applying said DC signal to resistance means (130);
- detecting a voltage drop over said resistance means (130) caused by said DC signal; and
- generating a voltage signal proportional to said detected voltage drop, said dynamic bias signal comprises said generated voltage signal.

22. The method according to any of the claims 19 to 21, **characterized in that** bias signal generating step comprises adjusting said dynamic bias signal for said second transistor (20).
